OPPORTUNITIES AND CHALLENGES FOR SPINTRONICS

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Conventional electronics use the flow of electric charges and are based on standard semiconductors. Spintronic devices exploit the electrons' spin to generate and control currents and to combine electric and magnetic signals. Today there is a strong effort worldwide to integrate spintronic devices with standard CMOS technology towards hybrid spin-CMOS chips, offering advantages in terms of power consumption, compactness, and speed. Recent results (from SAMSUNG [1], TSMC [2], etc.) confirm the merit of this approach.

In 2016, the Spintronics community decided to create the "SpinTronicFactory" (STF) network (www.SpinTronicFactory.eu) to promote European research and innovation in spintronics. The network, based on a legal Memorandum of Understanding, includes today 94 partners from 19 different countries. The role of STF is to consolidate the Spintronic community in Europe, to improve its visibility in Europe, and to increase the industrial impact of spintronic applications in the European Union. In 2020, a Roadmap for Spintronics was published [3]. A non-exhaustive list of key activities comprises sensors, spin-based technologies for ultra-low power applications, edge and in-memory computing, MRAMs and advanced sensors, beyond-CMOS logic, novel paradigms for computing, innovative hardware solutions for AI, rad-hard spin-based solution bringing novel functionalities to space applications, chiplets with spintronic technology, *etc.* Such high-performance, ultra-low power applications are key to enabling Europe's Digital Decade objectives, as well as its aspiration of reaching carbon neutrality in an ever-more digital environment.

Running projects

An important step for EU Spintronics has been the recent 2021 Horizon Europe call [4], nourishing Europe's long-term objective to reach its strategic autonomy in future enabling technologies. This funding aims to bring scientific excellence to higher TRL (TRL4-5): spin-based demonstrators will be developed in the coming years, integrating our technology with CMOS. Five projects have been granted, with a strong focus on magnonics, and other activities are ongoing in Europe (*e.g.*, several PathFinder projects, other Cluster 4 projects, *etc.*) spanning all spin-based activities promoted by STF. In the following, we will focus on those five granted projects.

MANNGA

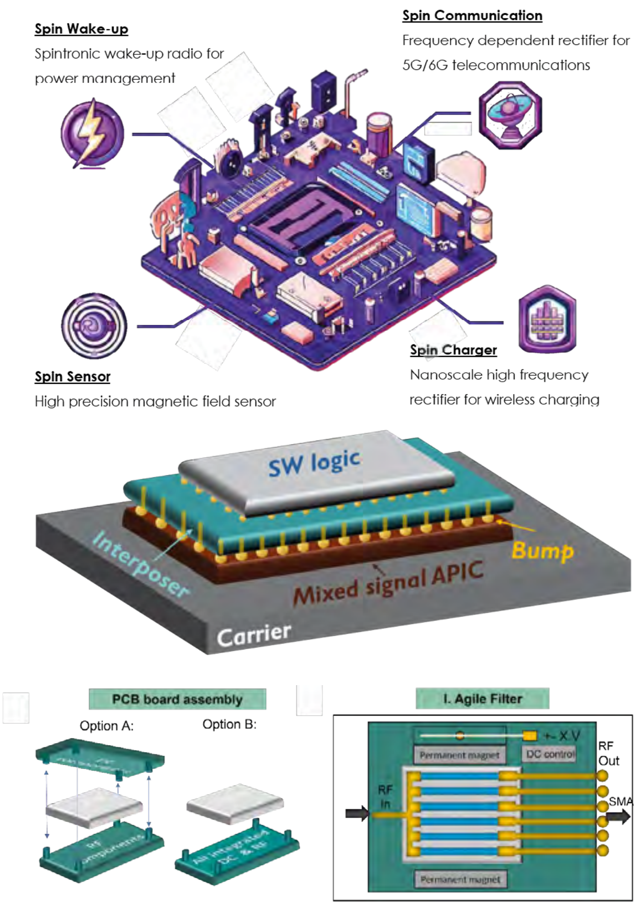
MANNGA [5] seeks to explore and challenge the limits of spin-based devices and their energy efficiency. This will be achieved by combining two inherently energy-efficient technology paradigms: (i) magnonics and (ii) neuromorphic computing. We will use nanoscale chiral magnonic resonators as building blocks of artificial neural networks. The power of the networks will be demonstrated by creating magnonics versions of field programmable gate arrays, reservoir computers, and recurrent neural networks. The ultimate efficiency of the devices will be achieved by (a) maximising their magnetic nonlinearity (via concentration of spin wave power within chiral magnonic resonators of minimal intrinsic loss); (b) using epitaxial YIG, which has the lowest known magnetic damping allowed by physics, for thin film magnonic media and resonators; (c) using wireless delivery of power (minimising Ohmic loss in interconnects). Sensitive to the resonators' micromagnetic states, such artificial neural networks will be conveniently programmable and trainable within existing paradigms of magnetic data storage.

M&MEMS

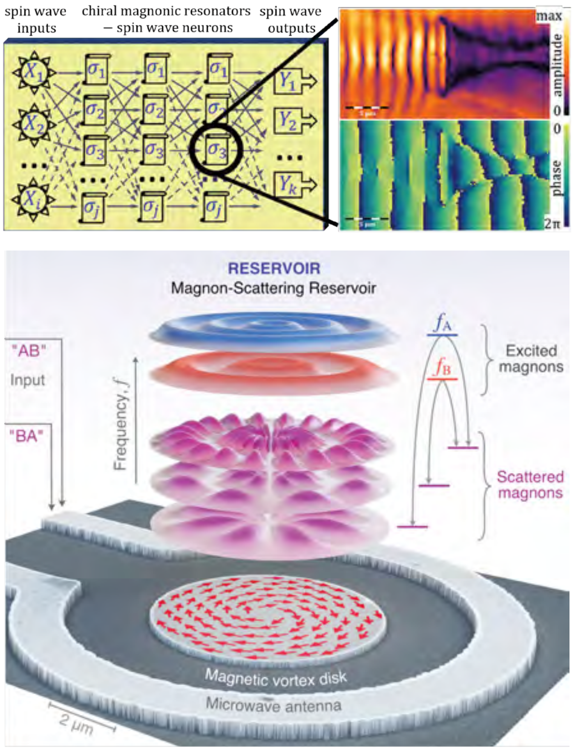
M&MEMS [6] aims at combining the tunability of magnonic systems with the power efficiency and agility of micro-electro-mechanical systems (MEMS). From the scientific side, the main goal of M&MEMS is to replace power-hungry electric currents as sources for static and dynamic magnetic fields. This is achieved by combining magnonic and MEMS devices on the same chip or in close proximity. These hybrid systems will enable a new generation of devices for radio-frequency (RF) communication and microwave signal processing. The consortium brings together research groups and industrial partners with a broad range of expertise in the fields of magnonics, MEMS, material science, and RF electronics. Two analog RF electronic functions have been identified: an agile filter with potential application in the field of 5G communication and beyond and a programmable phase shifter array, the building block of a novel directional antenna.

NIMFEIA

NIMFEIA [7] aims to provide a hardware solution for brain-inspired computing using magnetic materials on the nanoscale combined with advanced spintronics •••



▲ **FIG. 1:** Three examples of devices integrating Spintronic technology and CMOS. a) In the Swan-on-chip approach a wireless sensor node is fabricated implementing magnetic tunnel junctions directly on CMOS chips; different modules performing complex actions (sensing, communicating and power managing) are presented. b) In the SPIDER approach the spin-chip, responsible for the logic operation via spin-wave computing, is integrated via heterogeneous integration in package (RF interposer) with a mixed signal CMOS-based APIC (Analog Periphery Integrated Circuit). c) In the agile filter proposed by M&MEMS the spin-chip, where the radiofrequency filtering function is performed, is integrated with one (or two) PCBs responsible of the RF & DC parts; permanent magnets are directly integrated in the chip and their position is shifted by the MEMS.



▲ **FIG. 2: A schematic of a magnonic neural network developed by MANNGA project, and the response of its constituent neuron (a Fabry-Perot spin wave resonator) imaged by super-Nyquist time-resolved scanning Kerr microscopy. b) The magnon-scattering reservoir by the NIMFEIA project; image from the paper [10].**

● ● ● technologies. It is based on the disruptive idea of reciprocal space computing, utilising nonlinear interactions of quantised magnetic excitations. In the presence of nontrivial spin structures, such as magnetic vortices, these nonlinear interactions can be efficiently harnessed for reservoir computing tasks like pattern recognition and time series prediction with minimal pre-processing of input data. By making use of quantum interactions in reciprocal space, computing is done in individual spatially confined devices, such as a single magnetic disc, without the need to transport information data in real space.

SPIDER

SPIDER [8] targets a first benchmark of spin-wave computing at the system level. Spin wave computing is a disruptive spintronic technology that uses the interference of spin waves for computation and has considerable potential for power and area reduction per computing throughput, but despite much recent progress in the realisation of spin wave logic gates, no concept for a complete computing system exists today that is based only on spin waves. Thus, to advance from devices to systems, spin wave devices need to be complemented by CMOS in a hybrid spin wave–CMOS system. Using an interdisciplinary approach joining partners with expertise in materials science, physics, device manufacturing, electrical engineering, circuit design, and packaging, SPIDER targets the demonstration of a complete operational hybrid spin wave–CMOS computing system. SPIDER will design mixed signal CMOS chips that can drive spin wave circuits and read out computation results. The spin wave and CMOS chips will then be combined on an interposer to obtain the final hybrid system.

SWAN-on-chip

In SWAN-on-chip [9] a low-power sensor node solution is proposed in the form of the spintronics wireless autonomous node (SWAN), with the potential to extend node lifetime, and reduce carbon footprint and costs. The final vision of the SWAN paradigm is to have many customisable interconnected nodes, which can be harnessing spintronics components or conventional electronics depending on the suitability of the task required. The SWAN-on-chip concept will be used to validate the 'spintronics technology accelerator' platform, where the spintronics equivalent circuit models (Spin-EC) and spintronics multi-project wafer (Spin-MPW) will create a European-level pathway for the fabrication of monolithically integrated hybrid Spintronic/CMOS technologies required for boosting devices up the spintronics value chain. This validation will take the form of three homogeneously CMOS integrated spin-chip modules developed and benchmarked in the context of low-power IoT nodes (namely magnetic field sensor, wireless power transfer, wake-up receiver).

Future actions and links with the European Commission

These interesting approaches show the strong position of European partners in this field, thanks to the EC funding. Those projects are only one part of a larger activity based on spin-based technology. The next step will be to directly integrate magnetic materials in the EU Pilot Lines and move towards applications and products. Our objective as a community is to reinforce the link with foundries and key industrial partners in the field (in the EU and abroad); building dedicated demonstrators will be the key asset to convince new industrial partners of our approach.

Indeed, the EC launched a large action to reinforce the position of Europe in the chip landscape; the EU Chip Act is a great example, as well as the creation of the Chip Joint Undertaking (from the previous KDT JU). The strategy of the European industrial actors for electronics in the short and long term is also well defined (ECS-SRIA 2023.pdf (ecssria.eu)) where the importance of spintronics as an emerging technology is well recognised. However, the place for emerging technologies such as spintronics in the EU Chip Act is still fragile and not sufficiently developed compared to other communities (photonics, quantum technology, neuromorphics, *etc.*). In 2023, STF launched a collaboration with the EMA (https://magnetism.eu/) and with the IEEE Magnetic Society (https://ieeemagnetics.org/) in order to define the position of magnetic materials (and related applications) in tomorrow's chip. A dedicated symposium has been organised at the Intermag conference in Sendai (https://2023.intermag.org/). A similar action is expected at the next JEMS conference in Madrid (https://www.jems2023.es/) and the TMAG2023 conference in Rome (https://www.petaspin.com/tmag2023/).

Conclusions

In 2024 it would be strategic to create a synergy with the EC (via the EU Chip Act). We are convinced that the EC should reinforce the role of emerging technologies such as spintronics in the supply chain of next-generation chips "made in Europe". Two complementary actions may be considered: integrating magnetic materials in the semiconductor's roadmaps and supply chain and reinforcing activities on heterogeneous integration and packaging for those novel technologies. On one side, we believe that the EC should support the TRL ramp-up for projects, including those already funded. This will be naturally done both via already existing instruments (*i.e.* EIC Transition, EIC Accelerators, KDT, *etc.*) and via dedicated future calls in Cluster 4 (Innovation Actions, TRL 3 → TRL 6) on "Advanced Spintronics". These targeted actions will definitely reduce the time-to-market, providing Europe a first-mover advantage in this key enabling technology. At the same time, it is important to nourish the long-term applications 5-10 years from now. It is thus key to consider low-TRL calls providing alternatives to already existing solutions for spintronics, in the same logic of recent calls for Quantum Technologies [11]. The STF community is ready to take the challenge and launch new actions to bring spintronics into the EU products of tomorrow. ■

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